

ADAPTIVE SLOPE COMPENSATION FOR SWITCHING REGULATORS

Related Application

This patent application is a continuation-in-part of U.S. Patent
5 Application No. 10/703,960, which was filed November 7, 2003, and claims the benefit
under 35 U.S.C. 120 of the filing date.

Field of the Invention

The present invention relates to a system and method for adaptively
adjusting parameters in a switching regulator based on a slope that is associated with an
10 inductor in the switching regulator. The adaptive adjustment method is appropriate for
use in a switching regulator such as a buck regulator, a boost regulator, or a buck-boost
regulator.

Background of the Invention

Opposite polarity pulses can be applied to a transformer in a pulse-
15 width-modulated (PWM) power converter. The secondary winding of the transformer
is connected to additional circuitry such as a passive filter to generate an average output
voltage. The average output voltage is related to the pulse-width by the volts-seconds
rule and the characteristics of the transformer.

An example push-pull type PWM converter is illustrated in FIGURE 1.
20 As illustrated in FIGURE 1, transformer T1 conducts current (IC1, IC2) from the BP
power supply terminal through transistors Q1 and Q2. For example, the primary
winding of transformer T1 conducts current IC1 when transistor Q1 is activated, while
the primary winding of transformer T1 conducts current IC2 when transistor Q2 is
activated. Diodes D1 and D2 operate on opposite polarity cycles to provide current
25 (either ID1 or ID2) through inductor L to a load (not shown). Capacitor C0 is filter
ripple in the output voltage (VO).

Ideally, transistors Q1 and Q2 are activated for equal amounts of time
via drive signals DRV1 and DRV2 such that the volt-second integral of the pulses

applied to the transformer corresponds to zero and the transformer core does not saturate. However, non-ideal switching times for transistors Q1 and Q2 may result in unequal cycle times such that the transformer core is driven into saturation. Core saturation in a PWM converter may result in secondary effects such as breakdown in the switching transistors (Q1, Q2), excessive voltage and current stress on the rectifier diodes (D1, D2), as well as EMI related problems.

Brief Description of the Drawings

Non-limiting and non-exhaustive embodiments of the present invention are described with reference to the following drawings.

FIGURE 1 is an illustration of a conventional push-pull type PWM converter.

FIGURE 2 is an illustration of an example embodiment of a switching converter;

FIGURE 3 is an illustration of example waveforms for a switching converter;

FIGURE 4 is an illustration of a procedural flow for an example measurement system;

FIGURE 5 illustrates another example embodiment of a switching converter with analog differentiator processing system;

FIGURE 6 illustrates an example of a digital processing circuit;

FIGURE 7 illustrates an example block diagram of a dynamic slope adjustment mechanism for a buck or buck-boost type regulator;

FIGURE 8 illustrates an example schematic diagram for a circuit that is arranged to operate in accordance with the described block diagram illustrated by

FIGURE 7;

FIGURE 9 illustrates an example block diagram (900) of a dynamic slope adjustment mechanism for a boost type regulator;

FIGURE 10 illustrates an example schematic diagram for a circuit that is arranged to operate in accordance with the described block diagram illustrated by

FIGURE 9;

FIGURE 11 illustrates an example schematic diagram for a ramp generator circuit; and

FIGURE 12 illustrates another example schematic diagram for a ramp generator circuit, arranged in accordance with aspects of the present invention.

5 **Detailed Description of the Preferred Embodiment**

Various embodiments of the present invention will be described in detail with reference to the drawings, where like reference numerals represent like parts and assemblies throughout the several views. Reference to various embodiments does not limit the scope of the invention, which is limited only by the scope of the claims
10 attached hereto. Additionally, any examples set forth in this specification are not intended to be limiting and merely set forth some of the many possible embodiments for the claimed invention.

Throughout the specification and claims, the following terms take at least the meanings explicitly associated herein, unless the context clearly dictates
15 otherwise. The meanings identified below are not intended to limit the terms, but merely provide illustrative examples for the terms. The meaning of "a," "an," and "the" includes plural reference, the meaning of "in" includes "in" and "on." The term "connected" means a direct electrical connection between the items connected, without any intermediate devices. The term "coupled" means either a direct electrical
20 connection between the items connected or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means either a single component or a multiplicity of components, either active and/or passive, that are coupled together to provide a desired function. The term "signal" means at least one current, voltage, charge, temperature, data, or other signal.

25 Briefly stated, the invention is related to a system, method, and apparatus for providing adaptive slope compensation in a switching regulator that includes an inductor. A control loop of the switching regulator is responsive to a ramp signal. A ramp generator that includes a capacitor circuit and a current source provides the ramp signal, where at least one of the current level of the current source and the value of the
30 capacitor circuit are adjusted to vary the slope of the ramp signal. The adjustment of

the ramp signal is responsive to at least one of: a set point for the output voltage of the switching regulator, a feedback voltage that is related to the output voltage, and a measured parameter associated with the inductor in the switching regulator. By dynamically adjusting the slope of the ramp signal, slope compensation is provided for a range of inductor values that can dynamically change during operation.

Measured Inductor Characteristics

Inductors in switching electronic circuits are typically made out of ferrites or some other core material that has a higher permeability than air. Unlike air core inductors, the amount of current flowing in these inductors is constrained by the quality and quantity of the core material. Once the inductor's operating current exceeds a saturation point, the inductor's effectiveness is reduced and the rate of increase in the current relative to the applied voltage rises measurably. The inductor voltage (V_L) and the inductor current (I_L) are related to one another by: $\Delta I_L / \Delta t = \Delta V_L / L$.

Magnetic load applications such as motor drivers and switched-mode power supplied (SMPS) incorporate current limiting circuits to protect the control circuits (e.g., drivers, inductive elements, etc.) from currents that are sufficient to cause saturation and induce destructive currents. For example, in a SMPS the saturation current should always be greater than the current limit in the controller.

The various measurements of voltages and/or currents can be used to calculate values of characteristics associated with the inductor. Example characteristics include: inductor value, series resistance, slew rate in non-saturation, slew rate in saturation, average operating current, as well as others. Inductors with different core materials have different characteristic curves (e.g., the saturation and non-saturation slew rates change based on the type of core material) such that the type of core material and the value of the inductor can be determined (e.g., a lookup table that identifies the core material type based on characteristic measurements). The characteristic measurements can also be used in a control system such as in a switching-type converter (or regulator) to adaptively change control parameters such as: current limit, switching time, small signal compensation, and slope compensation.

Conventional circuits often include compensation to prevent undesirable effects such as oscillations, or some other instability or non-linearity in the control loop. In the present invention, characteristics associated with the inductor are measured and various control parameters associated with compensation of the circuit are dynamically
5 adjusted by the control circuit to accommodate a wide range of inductor values and saturation ratings. In one example, a parameter in the control loop is dynamically adjusted (e.g., additional current sources are enabled, a feedback amount is changed, a gain is adjusted, etc.) to change the compensating ramp associated with the inductor. In another example, a parameter in the control loop is dynamically adjusted based on the
10 rate of discharge in the inductor to change the slope compensation for the inductor.

FIGURE 2 is an illustration of an example embodiment of a switching converter (200) that is arranged according to an aspect of the present invention. Switching converter 200 includes an inductor (L), a switching transistor (T_{SW}), a diode (D_S), a capacitor (C_O), a load circuit (Z_L), and a measurement and system control (MSC)
15 block.

Inductor L is charged when switching transistor T_{SW} is active. Inductor current (I_L) is delivered to capacitor C_O and load circuit Z_L via diode D_S when transistor T_{SW} is inactive. In a normal operating mode, the MSC block is arranged to actuate switching transistor T_{SW} such that inductor L is periodically charged. The MSC block
20 is further arranged to monitor the voltages and currents associated with inductor L when the switching converter 200 is operated in a measurement mode, and provides a measurement of the inductance value based on those measurements.

The change in inductor voltage (ΔV_L) is determined by monitoring the input voltage (V_{IN}) and the switch voltage (V_{SW}). In one example embodiment, the
25 change in inductor current ($\Delta I_L/\Delta t$) is determined by monitoring the change in voltage across the switching transistor (ΔV_{DS}) and calculating: $(\Delta I_L/\Delta t) = (\Delta V_{DS}/\Delta t)/r_{dson}$, where r_{dson} is the on resistance of switching transistor T_{SW} . An optional resistor (R_S) may be placed in series with switching transistor T_{SW} to facilitate measurement of the inductor current.

FIGURE 3 is an illustration of example waveforms for a switching converter such as that illustrated in FIGURE 2. Ideally, the inductor does not reach a saturation point and the inductor current (I_L) and the voltage across transistor T_{SW} (V_{DS}) changes linearly in proportion to the value of the inductor. The non-ideal effects of inductor saturation are also illustrated as the inductor current (I_L) and the voltage across transistor T_{SW} (V_{DS}) experience a measurable change in slope when the saturation points (P_1 and P_2) are reached. The voltage across resistor R_S (when found in circuit 200) has the same shape as V_{DS} .

FIGURE 4 is an illustration of a procedural flow for an example measurement system that is useful for the present invention. After the measurement mode is activated by some triggering event, processing continues at block 410 where the inductor is operated for one or more cycles. At block 420, voltages (e.g., V_{IN} , V_{SW} , V_{DS} , V_{RS} , etc.) associated with the inductor are monitored (420) while the inductor is operated. At block 430, the monitored voltages are recorded and/or used to detect the saturation point (depending on the circuit implementation). From decision block 440, the process returns to block 420 when additional monitoring is necessary. Processing continues to block 450 when no additional voltages need be monitored. At block 450 values associated with the inductor (e.g., inductance value, slew rate, saturation point, etc.) are calculated. The calculated values can be used by other circuits or systems to adjust one or more parameters (e.g., current limit, slope compensation, etc).

In one example, voltages are monitored by an analog-type circuit that detects the change in slope associated with the current and/or voltage associated with the inductor. In another example, the inductor voltages are monitored by an analog-to-digital converter. In this example, either the digital values can be recorded in a memory and later retrieved for calculation purposes, or the digital values can be evaluated in real time to determine the rate of change in the voltages. In a further example, the digital values can be processed (e.g., averaged, throwing out extreme values, filtered, etc.) over many operating cycles of the inductor to minimize the effects of noise and switching transients on the measurement values. The processing of the digital values can be

provided as a post-processing function or in real-time based on the processing power of the system implementation.

FIGURE 5 illustrates another example embodiment of a switching converter (500) that is arranged in accordance with an aspect of the present invention.

5 Switching converter 500 is a buck-type converter that includes a p-type transistor (T_P), and n-type transistor (T_N), drivers (DRV_P , DRV_N), a controller (CNTL), a differentiator (DIFF), a comparator (CP), an SR-type latch (LATCH), a decrement circuit (DECR), a high-side turn-off circuit (TOHS), an inductor (L), a capacitor (C_O), and a load circuit (Z_L).

10 The controller (CNTL) is arranged to provide drive signals D_H and D_L to drivers DRV_P and DRV_N , respectively. Driver DRV_P provides a gate control signal (G_P) to p-type transistor T_P , while driver DRV_N provides another gate control signal (G_N) to n-type transistor T_N . The p-type transistor (T_P) is arranged to operate as a high side switch that couples the inductor (L) to the high power source (V_S). The n-type transistor (T_N) is arranged to operate as a low side switch that couples the inductor (L)
15 to the low power source (e.g., GND). Capacitor C_O is coupled in parallel with load circuit Z_L . A feedback signal (FB) is provided from V_O to the controller (CNTL).

An example differentiator illustrated in FIGURE 5 includes a capacitor (C), a resistor (R), and an amplifier (A_V). The differentiator is arranged to monitor the
20 drain-source voltage (V_{DS}) of p-type transistor T_P and provide a signal (V_{DIFF}) that is proportional to $\Delta V_{DS}/\Delta t$. The signal (V_{DIFF}) is used to adjust parameters within the circuit such as, for example, small-signal compensation, slope compensation, and current limit.

FIGURE 6 illustrates an example of a digital processing circuit (600)
25 that is arranged in accordance with aspects of the present invention. The digital processing circuit (600) includes an analog-to-digital converter (ADC) circuit, a memory circuit, and a digital processing logic (DPL) circuit. The ADC circuit is activated by a trigger mechanism (TRIGG) and converts a series of measurement signals (ISNS, VSNS, etc) to a data stream (raw data). The data stream is received by

the memory circuit for storage. Data in the memory circuit can be retrieved by the DPL circuit for further processing.

In one example, the memory circuit stores sampled data points that are utilized to find the value of $\Delta V_{DS}/\Delta t$, where the DPL circuit is arranged to calculate the value after all of the sampled points are stored. In another example, the memory circuit stores values that correspond to an average value, and the DPL circuit calculates a running average. The DPL circuit can further be arranged to: locate the saturation point of the inductor, calculate the slope of the inductor current, filter noise from the sampled data, discard anomalous data from the sampled data points, determine an appropriate current limit, determine a slope compensation parameter(s), determine a small-signal compensation parameter(s), as well as provide other calculations.

Slope Compensation Generally

Current mode control topologies can be applied to buck, boost, buck-boost, and other switching type converters/regulators. One example conventional buck regulator is operated at a fixed frequency with current mode control that includes peak current sensing for the inductor. Non-ideal effects are observed in this example regulator such as: an instability for duty cycles above 50%, poor loop response as the result of peak sensing instead of average inductor current, tendencies towards sub-harmonic oscillations, and poor noise sensitivity. The above-described instabilities are independent of regulator topology and may occur even when the voltage regulation loop is operated open loop. These and other non-ideal effects are addressed by adaptively adjusting the slope of the compensating ramp that is associated with the inductor current in accordance with the present invention.

According to an example of the present invention, a timing ramp is introduced into the current programming control loop. The slope of the inductor current determines the preferred amount of compensation that is provided by the slope (m_e) of the timing ramp. According to the present invention, the slope of the ramp (m_e) is related to a slope of the inductor current according to a scaling factor. In one example, the slope of the ramp (m_e) corresponds to a fraction of the downward slope associated

with the inductor current (m_2). In another example, the slope of the ramp (m_e) corresponds to a multiple of the downward slope associated with the inductor current (m_2). In yet another example, the slope of the ramp (m_e) is matched to the downward slope associated with the inductor current (m_2).

5 The topology selected and the desired optimization factor for the converter/regulator will dictate the selection of the scaling factor. The value of the downward slope of the inductor current (m_2) depends on the regulator topology, the value associated with the inductor, as well as other system parameters. An example buck or buck-boost regulator may have a downward slope (m_2) that is determined by the
10 ratio of the output voltage (V_{OUT}) and the inductor value (L) as: $m_2 = V_{OUT} / L$. In contrast, an example boost regulator may have a downward slope (m_2) that is related to the inductor value (L), and the difference between the input voltage (V_{IN}) and the output voltage (V_{OUT}) as: $m_2 = (V_{OUT} - V_{IN}) / L$. In each case, the downward slope (m_2) is inversely proportional to the value associated with the inductor (L).

15 The value associated with the inductor (L) can vary during operation. This is largely the result of the various materials that are used in the inductor. Many power inductors are built with a core material that exhibits some change in permeability with flux density. The flux density depends on the magnitude of operating current in the inductor. In a regulator system, the inductor current is largely dependent on the load
20 current for the system. Since the load current may change over time, the flux density of the inductor will change accordingly. Moreover, it may be desirable to support a range of inductor values so that the system designer for the regulator is afforded some flexibility in design and suppliers for the inductors.

 As described previously, a measurement signal can be generated that is
25 proportional to a value associated with the inductor (L). According to the present invention, the measurement signal can be used to adjust the slope of the compensation ramp (m_e) to compensate for changes in L . By dynamically adjusting the slope of the compensation ramp (m_e), large variations in the inductance value (L) can be accommodated without changing the internal constants of the regulator.

30

Example Slope Compensation Mechanism for Buck and Buck-Boost Type Regulators

FIGURE 7 illustrates an example block diagram (700) of a dynamic slope adjustment mechanism for a buck or buck-boost type regulator that is arranged according to an aspect of the present invention. The block diagram includes three gain blocks (710, 720 and 730), a divider block (740), and a ramp generator block (750).
5 Although illustrated as separate functional blocks, the functions illustrated in block diagram 700 can be combined and/or separated as may be desired in a particular implementation.

The first gain block (710) is arranged to: receive an input signal (V_{REF}) that is proportional to the output voltage (V_{OUT}) of the regulator, and provide a scaled signal that is related to the input signal (V_{REF}) according to a first constant (K_R). The second gain block (720) is arranged to: receive an input signal (V_I) that is proportional to the value of the inductor (e.g., by measuring the inductor value as previously described), and provide a scaled signal that is related to the input signal (V_I) according to a second constant (K_I). The divider block (740) is arranged to: receive the scaled signals from the first and second gain blocks via terminals X and Y, and provide a ratio signal that is proportional to the ratio of the signals from the X and Y terminals (e.g., $Z=X/Y$). The third gain block (730) is arranged to: receive the ratio signal (e.g., X/Y) from the divider block, and provide a scaled signal that is related to the ratio signal according to a third constant (K). The ramp generator block (750) is arranged to:
10 receive the scaled signal from the third gain block, and provide a ramp signal (e.g., RAMP) that has a slope corresponding to m_e . The ramp generator block can optionally include another gain scaling coefficient that corresponds to K_e .
15

In one example, signal V_{REF} is a constant signal that represents the desired output voltage (e.g., V_{OUT}) of the regulator. In another example, signal V_{REF} is a signal that is directly proportional to the output voltage (e.g., V_{OUT}) of the regulator through some kind of feedback arrangement (e.g., a resistor divider).
20
25

The slope (m_e) of the ramp signal (e.g., RAMP) can be mathematically expressed as:

$$m_e = \frac{V_{REF}}{V_I} \cdot \frac{(K_R \cdot K \cdot K_e)}{K_I} \quad (\text{Eq.1})$$

As described previously, the downward slope associated with the inductor current in a buck or buck-boost regulator can be expressed as:

$$m_2 = \frac{|V_{OUT}|}{L} \quad (\text{Eq.2})$$

Since signal V_{REF} is proportional to the output voltage (V_{OUT}) and signal V_I is proportional to the value of the inductor (L), the value associated with the slope (m_e) of the ramp signal (RAMP) will track changes in the downward slope (m_2) of the inductor current (e.g., I_L). The various constants associated with the above-described function blocks (e.g., K , K_e , K_R and K_I) can be adjusted to set the desired proportionality between slopes m_e and m_2 . According to the described slope adjustment method, the compensation ramp slope can be adjusted to compensate for the effects of variations in inductance values, and other parameters associated with the inductor current (e.g., V_{IN} , V_{OUT} , and load conditions).

FIGURE 8 illustrates an example schematic diagram for a circuit (800) that is arranged to operate in accordance with the described block diagram illustrated by FIGURE 7. The example circuit includes nine transistors ($Q_1 - Q_9$), three current sources ($I_1 - I_3$), a capacitor (C), and a resistor (R).

Transistors Q_1 and Q_2 are arranged in a current-mirror configuration, where transistor Q_1 is arranged to sense the current from current source I_1 , which has an operating current given by: $I_1 = V_{REF} \cdot K_R \cdot K_I$. Transistors Q_2 and Q_3 are arranged to cooperate with one another to provide a common control signal to transistors Q_4 and Q_5 . Transistor Q_4 is arranged to cooperate with current source I_3 , which is biased to provide current I_{BIAS} to transistors Q_3 and Q_4 . Transistor Q_5 is arranged to cooperate with current source I_2 , which has an operating current given by $I_2 = V_I \cdot K_I \cdot K_I$. Transistor Q_6 is responsive to the signal provided by transistor Q_5 and current source I_2 . Transistors Q_7 and Q_8 are arranged in a current-mirror configuration, where transistor Q_7 senses the

current from transistor Q₆ and transistor Q₈ provides a scaled current according to scaling factor K. Transistor Q₉ is responsive to a clock signal (CLOCK) via resistor R such that the ramp signal (RAMP) is reset to a ground potential when transistor Q₉ is active. Capacitor C is arranged to receive the current from transistor Q₈ when transistor

5 Q₉ is inactive such that the ramp signal is provided as a voltage across capacitor C.

The current ($V_{REF} \cdot K_R \cdot K_I$) associated with current source I₁ is proportional to the output voltage (V_{OUT}) through signal V_{REF}, while the current ($V_I \cdot K_I \cdot K_I$) associated with current source I₂ is proportional to the value of the inductance (L) of the power inductor. Transistors Q₃, Q₄, Q₅, and Q₆ are arranged to
 10 operate as a current divider that is responsive to currents I₁ and I₂. The output of the current divider is provided at the collector of transistor Q₆. The current mirror ratio for transistors Q₇ and Q₈ corresponds to (1:K), where K is a constant that can control the rate (slope) of the ramp signal (RAMP). The ramp generator portion of the circuit includes the collector current of transistor Q₈ and the value associated with capacitor C.
 15 Since the slope of the voltage across the capacitor is equal to I_{C8}/C, where I_{C8} is the current from Q₈, the ramp signal (RAMP) has a slope (m_e) that is given by:

$$m_e = \frac{V_{REF}}{V_I} \cdot \frac{(K_R \cdot K)}{K_I} \cdot \frac{I_{BIAS}}{C} \quad (Eq.3)$$

Eq.3 is in substantially the same form as Eq.2 such that adjustment of various constants can be employed to adjust the slope of the ramp signal as previously
 20 described.

Example Slope Compensation Mechanism for Boost Type Regulators

FIGURE 9 illustrates an example block diagram (900) of a dynamic slope adjustment mechanism for a boost type regulator that is arranged according to an
 25 aspect of the present invention. The block diagram includes four gain blocks (910, 920, 930 and 940), a difference block (950), a divider block (960), and a ramp generator block (970). Although illustrated as separate functional blocks, the functions illustrated in block diagram 900 can be combined and/or separated as may be desired in a particular implementation.

The first gain block (910) is arranged to: receive an input signal (V_{REF}) that is proportional to the output voltage (V_{OUT}) of the regulator, and provide a scaled signal that is related to the input signal (V_{REF}) according to a first constant (K_R). The second gain block (920) is arranged to: receive an input signal (V_{IN}) that is proportional to the input voltage of the regulator, and provide a scaled signal that is related to the input signal (V_{IN}) according to a second constant (K_V). The third gain block (930) is arranged to: receive an input signal (V_I) that is proportional to the value of the inductor (e.g., by measuring the inductor value as previously described), and provide a scaled signal that is related to the input signal (V_I) according to a third constant (K_I). The difference block (950) is arranged to receive the scaled signals from the first and second gain blocks and provide a difference signal (V_{DIFF}) that is proportional to the difference between signals V_{REF} and V_{IN} . The divider block (960) is arranged to: receive the scaled signals from the difference block and third gain blocks via terminals X and Y, and provide a ratio signal that is proportional to the ratio of the signals from the X and Y terminals (e.g., $Z=X/Y$). The fourth gain block (940) is arranged to: receive the ratio signal (e.g., X/Y) from the divider block, and provide a scaled signal that is related to the ratio signal according to a fourth constant (K). The ramp generator block (970) is arranged to: receive the scaled signal from the fourth gain block, and provide a ramp signal (e.g., RAMP) that has a slope corresponding to m_e . The ramp generator can optionally include another gain scaling coefficient that corresponds to K_e .

In one example, signal V_{REF} is a constant signal that represents the desired output voltage (e.g., V_{OUT}) of the regulator. In another example, signal V_{REF} is a signal that is directly proportional to the output voltage (e.g., V_{OUT}) of the regulator through some kind of feedback arrangement (e.g., a resistor divider).

The slope (m_e) of the ramp signal (e.g., RAMP) can be mathematically expressed as:

$$m_e = \frac{(V_{REF} \cdot K_R - V_{IN} \cdot K_V)}{V_I} \cdot \frac{(K \cdot K_e)}{K_I} \quad (\text{Eq.4})$$

As described previously, the downward slope associated with the inductor current in a boost regulator can be expressed as:

$$m_2 = \frac{V_{OUT} - V_{IN}}{L} \quad (\text{Eq.5})$$

Since signal V_{REF} is proportional to the output voltage (V_{OUT}), signal V_1 is proportional to the value of the inductor (L), and signal $V_{IN} \cdot K_V$ is proportional to the input voltage (V_{IN}), the value associated with the slope (m_e) of the ramp signal (RAMP) will track changes in the downward slope (m_2) of the inductor current (e.g., I_L). The various constants associated with the above-described function blocks (e.g., K , K_e , K_R , K_V and K_I) can again be adjusted to set the desired proportionality between slopes m_e and m_2 . According to the described slope adjustment method, the compensation ramp slope can be adjusted to compensate for the effects of variations in inductance values, and other parameters associated with the inductor current (e.g., V_{IN} , V_{OUT} , and load conditions).

FIGURE 10 illustrates an example schematic diagram for a circuit (1000) that is arranged to operate in accordance with the described block diagram illustrated by FIGURE 9. Example circuit 1000 includes nine transistors ($Q_1 - Q_9$), four current sources ($I_1 - I_4$), a capacitor (C), and a resistor (R). FIGURE 10 is substantially the same as FIGURE 8 with the addition of current source I_4 , which is coupled to the collector of transistor Q_1 . Current source I_4 is arranged to provide a current that corresponds to $I_4 = V_{IN} \cdot K_V \cdot K_I$. With the addition of current source I_4 , the collector current (I_{C1}) of transistor Q_1 corresponds to:

$$I_{C1} = I_1 - I_4 = (V_{REF} \cdot K_R \cdot K_I) - (V_{IN} \cdot K_V \cdot K_I) \quad (\text{Eq.6})$$

As described before, with respect to Eq.3, the voltage across the capacitor is determined by I_{C8}/C . However, since current source I_4 is included in FIGURE 10, current I_{C8} will include portions of current I_1 and I_4 through the various current mirror arrangements such that, the resulting ramp signal (RAMP) has a slope (m_e) that is given by:

$$m_e = \frac{(V_{REF} \cdot K_R - V_{IN} \cdot K_V)}{V_1} \cdot \frac{K}{K_I} \cdot \frac{I_{BIAS}}{C} \quad (\text{Eq.7})$$

Eq.7 is in substantially the same form as Eq.4 such that adjustment of various constants can be employed to adjust the slope of the ramp signal as previously described.

5 Example Capacitive Adjustment Mechanisms for Slope Compensation

As described above with respect to FIGURES 7 - 10, the slope of the inductor current is adjusted by changing the scaling constants associated with the various gain blocks. For example, the current mirror ratio as set by scaling constant K in FIGURES 8 and 10 can be varied to change the slope compensation of the inductor
10 current. Some alternative ways to scale the slope compensation are illustrated by FIGURES 11 and 12.

FIGURE 11 illustrates an example schematic diagram for a ramp generator circuit (1100) that is arranged to operate in accordance with an aspect of the present invention. The ramp generator circuit (1100) may be configured to operate as a
15 portion of the control circuit for the power switch in the switching regulator. Ramp generator circuit 1100 includes a decoder logic block (1110), an array of capacitor circuits (1120), and a current source (I).

A digital measurement signal is obtained in the system (e.g., see FIGURE 1), where the digital measurement signal corresponds to a measurement such
20 as a value for the inductor (or average value as may be desired) in the switching regulator. The digital measurement signal is provided to decoder logic block 1110, which is arranged to provide an array of digital control signals. Capacitor circuits 1120 are arranged as a set of selectable capacitors that are selectively coupled in parallel to one another based on the array of digital control signals from the decoder logic block
25 (1110). The effective total capacitance from the array of capacitor circuits operates as a single capacitive value for the ramp capacitor (C) in the ramp generator circuit, where the slope of the ramp is variable in response to the digital measurement signal.

FIGURE 12 illustrates another example schematic diagram for a ramp generator circuit (1200) that is arranged to operate in accordance with an aspect of the
30 present invention. The ramp generator circuit (1200) may be configured to operate as a

portion of the control circuit for the power switch in the switching regulator (e.g. see FIGURES 1 - 6 and related discussion). Ramp generator circuit 1200 includes a digital-to-analog converter (DAC) circuit that is responsive to a digital measurement signal (e.g., a measured value for the inductor). The DAC circuit is arranged to provide a
5 programmable output current to the capacitor in the ramp circuit such that the slope of the inductor current is adjusted.

The above specification, examples and data provide a complete description of the manufacture and use of the composition of the invention. Since many embodiments of the invention can be made without departing from the spirit and scope
10 of the invention, the invention resides in the claims hereinafter appended.